Amendments to the Specification:

Please replace paragraph beginning on page 10, line 7 with the following amended paragraph:

The configuration of the bus protocol that the device is compatible with is user selectable. This allows a peripheral device to be implemented on a chip to minimize cost. FIG. 5 shows a block diagram of a multi-mode wireless communicator device 100 fabricated on a single silicon integrated chip. The chip can be accessed or controlled by a host computer through either a PCI bus interface or a PCMCIA bus interface, both of which sharing one set of pins to conserve pin-out of the chip. In one implementation, the device 100 is an integrated CMOS device with radio frequency (RF) circuits, including a cellular radio core 110, a short-range wireless transceiver core 130, and a sniffer 111, along side digital circuits, including a reconfigurable processor core 150, a high-density memory array core 170, and a router 190. The high-density memory array core 170 can include various memory technologies such as flash memory and dynamic random access memory (DRAM), among others, on different portions of the memory array core. A multi-protocol interface bus 105 is connected to a bus linking the digital circuits so that a host computer can control and/or retrieve received data or transmit data using the wireless communicator device 100. Also shown in FIG. 5 the short-range wireless transceiver core 130 further includes a radio frequency (RF) core 132, which may be an RF modem core that communicates with a link controller core 134.